Cancellation of Capacitor Parasitic Parameters for Noise Reduction Application

Shuo Wang, *Member, IEEE*, Fred C. Lee, *Fellow, IEEE*, and Willem Gerhardus Odendaal, *Member, IEEE*

***Abstract*—In this paper, a method is proposed to reduce the equivalent series inductance and equivalent series resistance of capacitors. The method is, first, theoretically analyzed and then verified through experiments. This method will show that it can be used for both film capacitors and electrolytic capacitors, greatly improving the performance of both. Applications in practical power converters prove that the proposed technique can significantly reduce high frequency (HF) electromagnetic interference noise. The technique can also be very useful to reduce HF voltage ripple.**

***Index Terms*—Electromagnetic interference (EMI) filter, equivalent series inductance (ESL), equivalent series resistor (ESR), parasitic cancellation.**

I. Introduction

THE equivalent series inductance (ESL) plays a very important role on capacitor high frequency (HF) performance. As important components of power converters, capacitors' HF performance significantly affects the peak–peak value of noise which superposes on the voltage ripple at the converter's output and the HF conducted noise spectrum at the converter's input. It is well known that ESL and capacitance can resonate and make a capacitor perform like an inductor at HF range; therefore it is very important to reduce the ESL of capacitors. The capacitor performance is usually evaluated by the insertion voltage gain. The test setup and typical simulated insertion voltage gain are shown in Figs. 1 and 2.

Two curves are shown in Fig. 2. One is the insertion voltage gain for a capacitor and the second one is the insertion voltage gain when ESL is zero. f_S is the series resonant frequency of the capacitor and T_m is the lowest value of the transfer-gain. They are given through

$$f_S = \frac{1}{2\pi\sqrt{\mathrm{ESL}\times C}} \tag{1}$$

$$T_m \approx 20\times\log\left(\frac{\mathrm{ESR}}{25}\right). \tag{2}$$

If ESL is zero, the capacitor performance is significantly improved at HF range. The HF performance is determined by ESR only, and if ESR is reduced, HF performance can be further improved.

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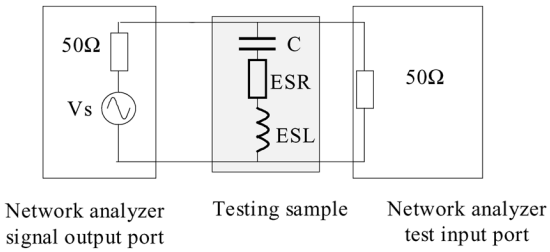

Fig. 1. Setup for evaluating the insertion voltage gain of a capacitor.

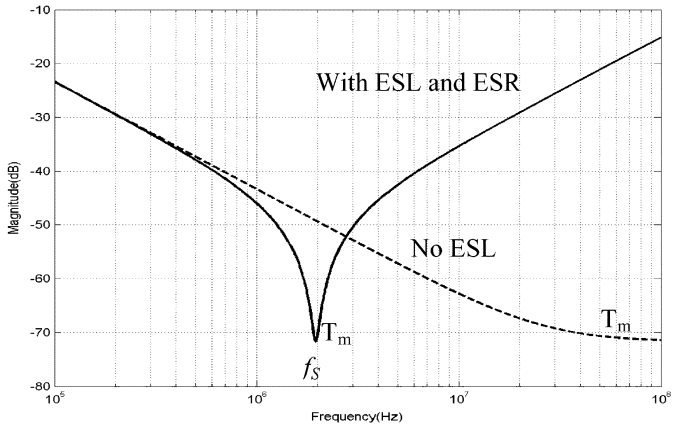

Fig. 2. Insertion voltage gain curves of capacitors.

In this paper, a method is proposed to reduce the effects of ESL and ESR, especially ESL, of capacitors. Experiments show that HF performance is greatly improved.

II. Network Theory of ESL and ESR Cancellation

For the network 1 shown in Fig. 3, it is well known that the port voltage and current satisfy the relationship defined by the Z matrix, which is shown in

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} \tag{3}$$

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0}; \quad Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0};$$
$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0}; \quad Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0}. \tag{4}$$

The $\mathbf{Z}$ matrix can therefore be calculated through (4) as

$$\mathbf{Z} = \begin{pmatrix} \frac{Z_2+Z_1}{2} & \frac{Z_2-Z_1}{2} \\ \frac{Z_2-Z_1}{2} & \frac{Z_2+Z_1}{2} \end{pmatrix}. \tag{5}$$

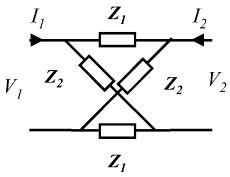

Fig. 3. Network 1.

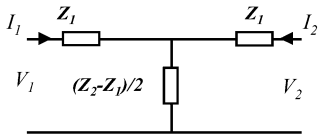

Fig. 4. Network 2.

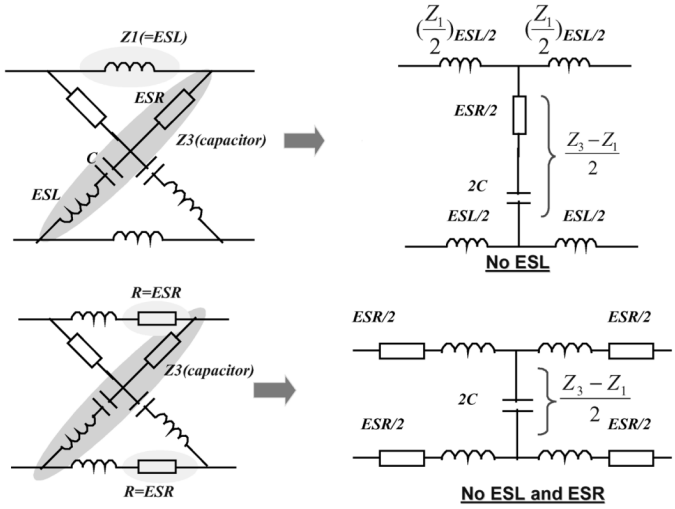

Fig. 5. ESL and ESR cancellation for capacitors.

In (3), Z_{11} is the input impedance of port1 when port2 is open. Because it is actually two impedances $Z_1 + Z_2$ in parallel, it results in $(Z_2 + Z_1)/2$ as shown in (5). Z_{22} is the same as Z_{11} since the network is symmetric. Z_{12} is the transfer-impedance between two ports which represents the effects of port2 on port1 in terms of impedance. It is given by the ratio of the voltage on port1 to the excitation current on port2 when port 1 is open. This results in $(Z_2 - Z_1)/2$ as shown in (5). Z_{21} is the same as Z_{12} since the network is considered as a passive linear network [2].

For the network 2, shown in Fig. 4, it can be proven that the Z matrix is also given by (5). Four impedances in the Z matrix can also be explained by their definitions similarly to above. Because these two networks have the same Z matrix, they are equivalent. Two networks thus have same characteristics on two ports. Comparing these two networks, the impedances Z_1 in the network 1 are actually subtracted from Z_2 and are pushed to the two sides of the signal paths, as shown in the network 2. Based on this observation, the ESL and ESR of two capacitors can be cancelled using extra inductors and resistors. This idea is shown in Fig. 5.

In Fig. 5, two capacitors are diagonally connected. The cancellation inductors and resistors are connected on the top and bottom sides. It is obvious that under the ideal conditions, if the cancellation inductance is equal to ESL, then the effects of ESL on the shunt path are cancelled. If cancellation resistance is equal to ESR, then the effects of ESR on the shunt path are cancelled. The resultant networks are equivalent to noise filters because the ESL and ESR are on signal paths and capacitance is on a shunt path.

It should be pointed out that, although ESR cancellation can reduce the effects of ESR, it may not be a good practice for large current application. For the resultant ESL and ESR cancellation network in Fig. 5, because two ESR are in the low frequency (LF) current path, LF current I, for example 60-Hz ac current, flows through the two ESRs. This will result in a loss of $2I^2$ ESR. If ESR is 10 mΩ, 10-A LF current can cause 2-W loss. On the other hand, ESL cancellation does not introduce extra losses for LF current. And at the same time, it provides a low impedance path, which is much lower than that which two parallel capacitors can provide, for HF noise current. ESL cancellation is therefore a good practice from dc to 30 MHz and from low current to high current applications.

ESR and ESL can not be totally cancelled, because they are the functions of temperatures, frequencies, and currents, however, they can be effectively reduced, thereby greatly improving the performance of the capacitors.

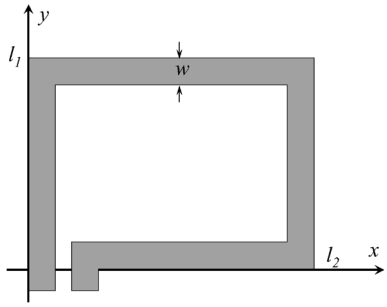

Fig. 6. One-turn rectangular PCB winding.

III. Experimental Results

A. Implementation on PCB

ESL is usually very small, so the cancellation inductors can be constructed using printed circuit board (PCB) windings or a piece of wire. The inductance for a rectangular PCB winding shown in Fig. 6 is given as [1]

$$L \approx \frac{\mu_0}{2\pi}\left[2l_2\ln\left(\frac{2l_2}{w}\right)+2l_1\ln\left(\frac{2l_1}{w}\right) - 2l_2\sinh^{-1}\left(\frac{l_2}{l_1}\right)-2l_1\sinh^{-1}\left(\frac{l_1}{l_2}\right) + 4\left(l_1^2+l_2^2\right)^{1/2}+(l_1+l_2) \times\left(\frac{1}{6}-\frac{2}{3}\ln 2-\frac{2\pi}{3}\right)\right] \quad (6)$$

where the thickness of the PCB winding is ignored.

The cancellation resistors are in series with the cancellation windings. Two capacitors are not necessarily placed like the pattern shown in Fig. 5. They can be placed side by side making the idea easy to implement in a practical PCB layout.

To implement the cancellation technique on a PCB is easy. In Fig. 7, two film capacitors are placed side by side on a PCB. The cancellation windings are realized using rectangular PCB windings. Cancellation resistors are soldered in series with the

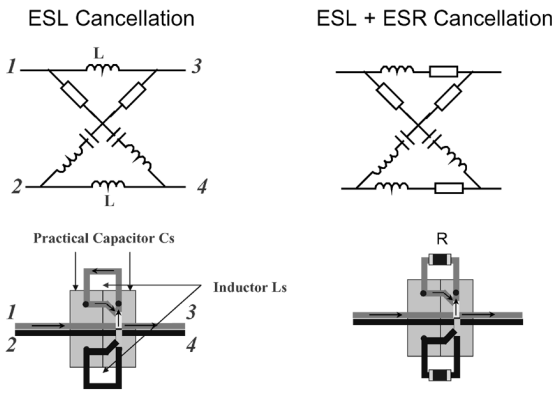

Fig. 7. Implementation of ESL and ESR cancellation on PCB.

PCB windings. For the design of cancellation turn in Fig. 6, w is determined by operation current and thickness of copper layer; l_2 is determined by the physical distance of two capacitors, and then l_1 is found through (6). The inductances to be cancelled include the ESL of capacitors and parasitic inductance of pins and PCB layout. The final l_1 and l_2 are tuned by conducting experiments because of the effects of parasitics on PCB. In order to keep stable cancellation inductance at different frequencies, no copper layers are allowed to be laid in and near the cancellation winding because the eddy currents, which are induced by the magnetic flux of cancellation turn, in these copper layers can partly cancel the inductance of the cancellation turns at high frequencies. The capacitance of the film capacitors in the experiment is 0.47 μF. Its ESL is 14 nH and ESR is 16 mΩ.

For electrolytic capacitors, the PCB layout is almost same, while for high current application, cancellation resistors may not be anticipated because of the loss they may introduce. The capacitance of the electrolytic capacitors in the experiment is 220 μF and its ESL is 15 nH. The voltage rating is 250 V.

The prototypes are shown in Figs. 8 and 9.

B. Measurement Results

The prototype with film capacitors is first measured. Measurements are carried out in both frequency and time domains. The equivalent measurement setup for time domain is shown in Fig. 10 and the measured waveforms are shown in Fig. 11.

In Fig. 11, the signal generator's output is a 10-MHz sinusoidal wave with a 19.4-V peak-to-peak value. Two measurements are then conducted. The first measures the output voltage of two parallel film capacitors. The cancellation prototype with the film capacitors is measured with the second measurement. From Fig. 11, after ESL is cancelled, the voltage ripple (10 MHz) on capacitors is smaller than 10 mV. This is much smaller than 170 mV in the case without the cancellation because the self resonant frequency of the capacitor is around 2 MHz.

The equivalent measurement setup for frequency domain is shown in Fig. 12 and measured insertion voltage gains are shown in Fig. 13.

Three curves are shown in Fig. 13. The first curve is the two parallel film capacitors, the second curve is ESL cancellation and the last curve is both ESL and ESR cancellation. This shows that after ESL is cancelled, a 25-dB improvement is achieved at 30 MHz. Fig. 13 also shows that, after ESR is reduced, improvement at high frequency range is further increased to 27 dB. Because ESR is just an equivalent loss of capacitors, it is the function of many parameters. As a result, ESR cancellation is not as good as we expected.

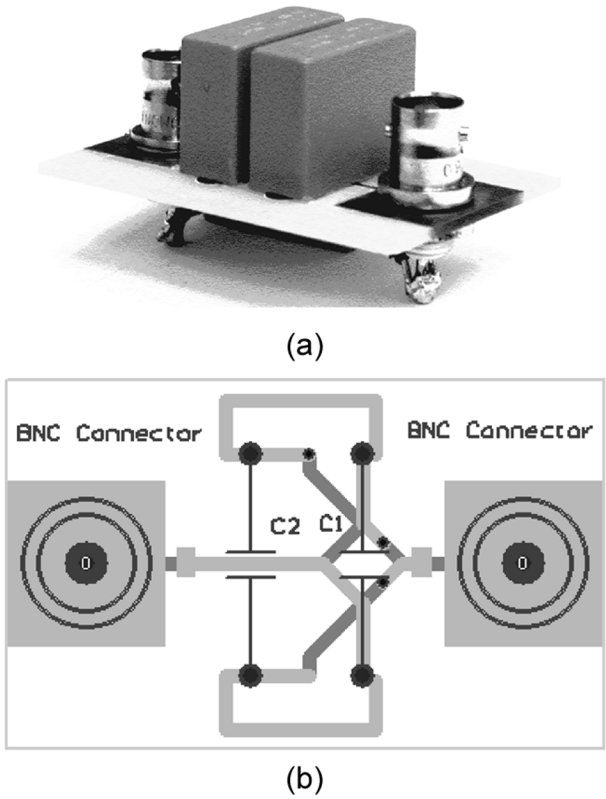

Fig. 8. Implementation for two 0.47-μF/400-V film capacitors: (a) prototype and (b) PCB layout.

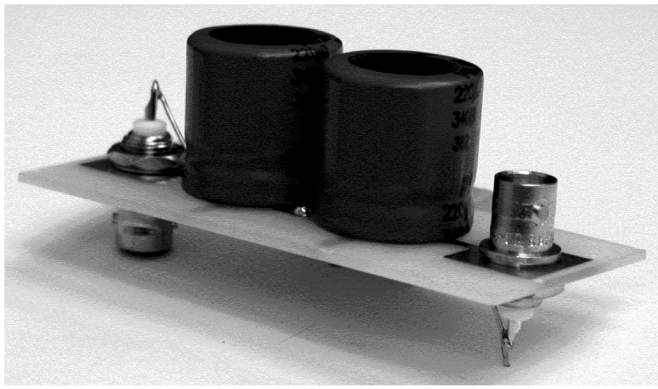

Fig. 9. Implementation for two 220 μF/250-V electrolytic capacitors.

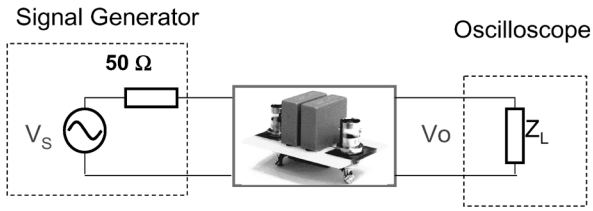

Fig. 10. Equivalent measurement setup for the prototype with film capacitors in time domain.

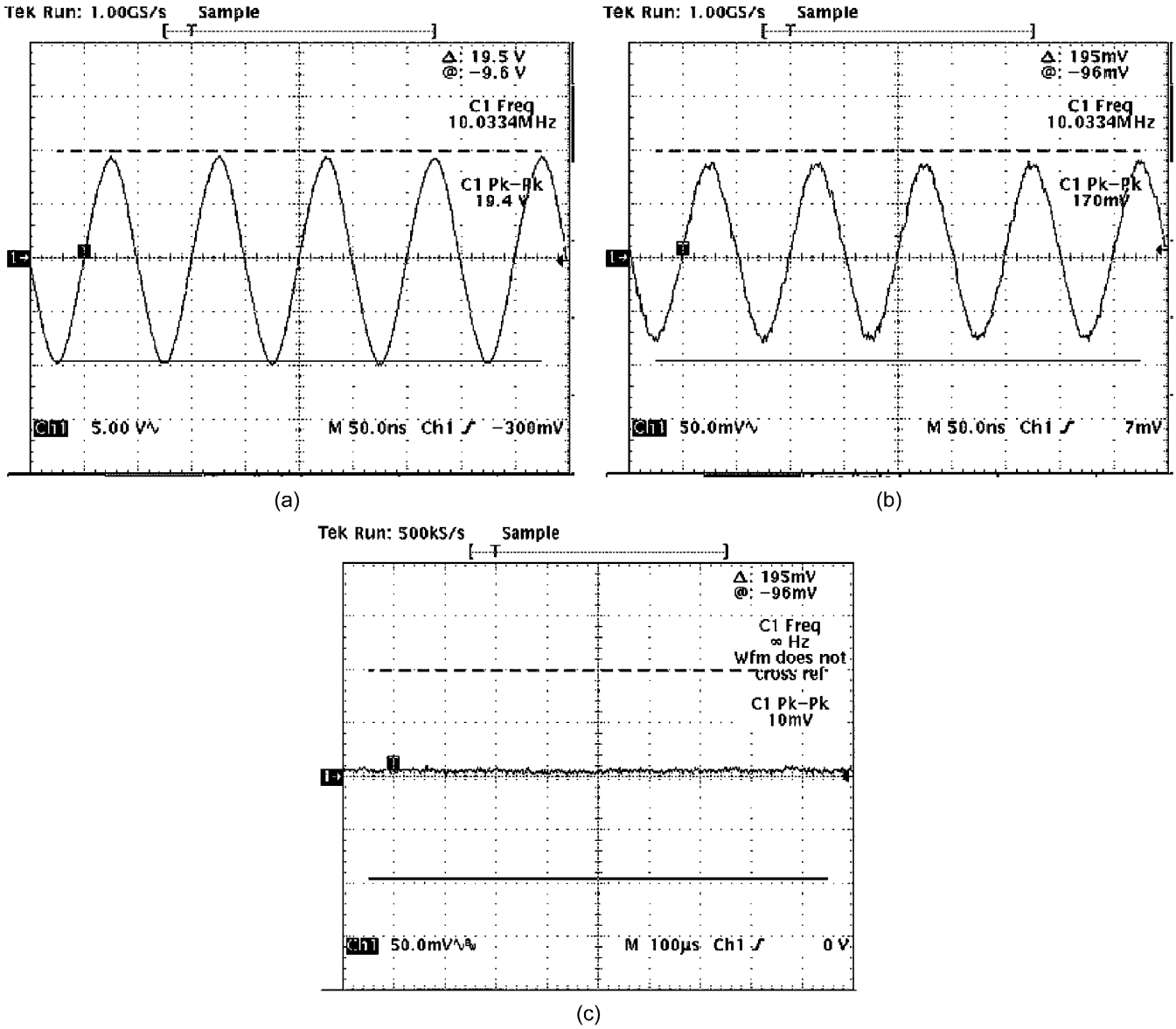

Fig. 11. Comparison of measured results for the prototype with film capacitors. (a) Input voltage ripple. (b) Voltage ripple of two parallel capacitors. (c) Voltage ripple of ESL cancelled capacitors.

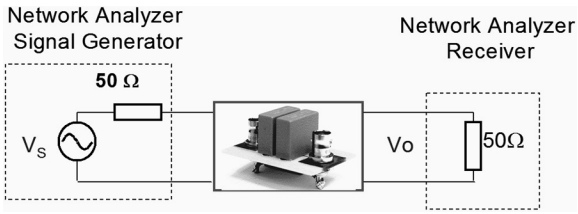

Fig. 12. Equivalent measurement setup for the prototype with film capacitors in frequency domain.

The bump between 10 MHz and 20 MHz is caused by the transmission line structure of film capacitors [3], which makes capacitor HF performance worse and ESL cancellation not as good as we expected.

Fig. 14 shows the measured insertion voltage gains for the prototype of electrolytic capacitors. This figure also shows that the performance of electrolytic capacitors in HF range (above 1 MHz) is greatly improved. The prototype's performance at 30 MHz is factually almost the same as it would be at 100 kHz, which implies no extra small HF capacitors are needed to parallel with them. The prototype achieved more than 27-dB improvement at 30 MHz compared to the one without ESL cancellation. The self-resonant frequency of investigated electrolytic capacitors is lower than 100 kHz, so the curve shape is different from the cases in Fig. 2, Fig. 13, and (2) explain the flat frequency response. Because ESL is cancelled, only ESR affects capacitor performance, resulting in a frequency response that is flat. Because electrolytic capacitors are usually used for output and input filters in converters, high frequency current and voltage ripples can be significantly reduced.

C. Application to Noise Filters

When the proposed method is used in a Γ (LC) type EMI filter, as shown in Fig. 15, much attention should be paid to

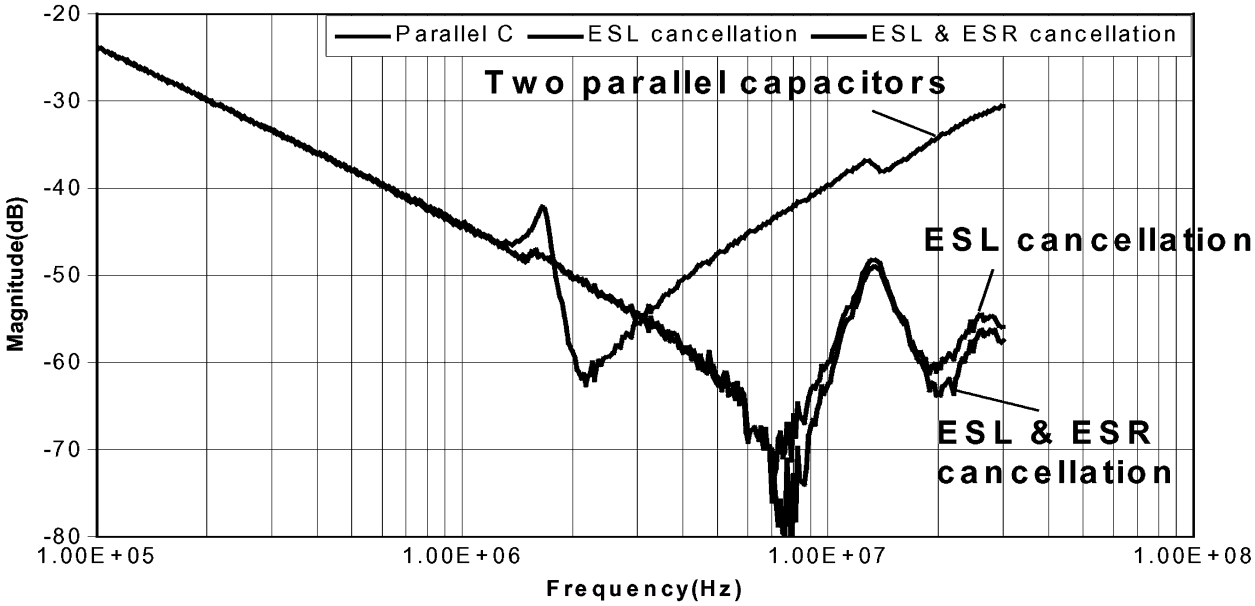

Fig. 13. Comparison of insertion voltage gains for the prototype with film capacitors.

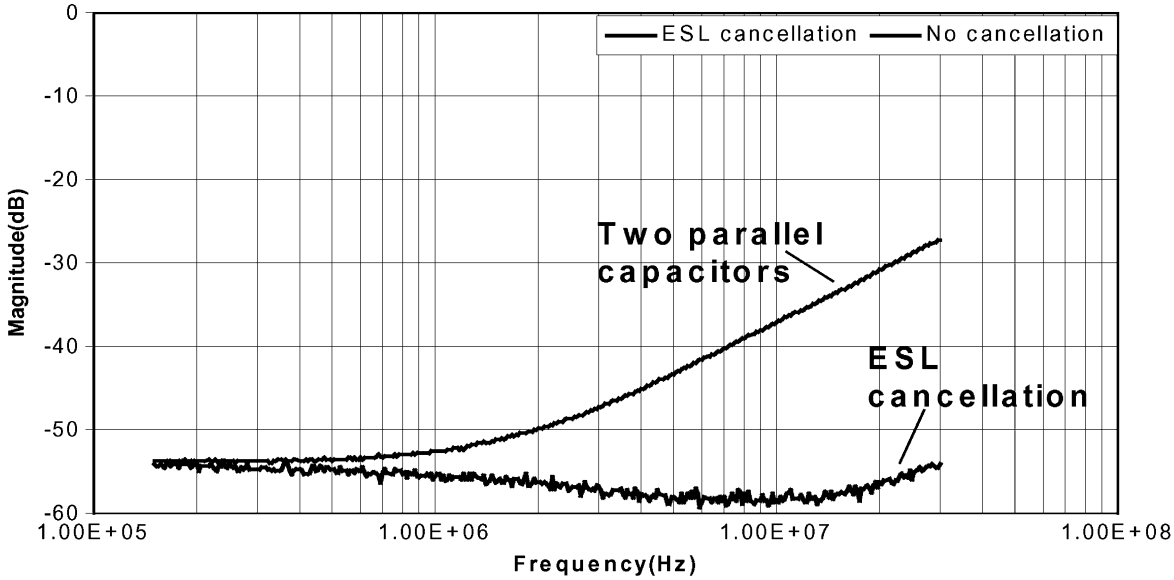

Fig. 14. Comparison of insertion voltage gains for the prototype with 220-μF/250-V electrolytic capacitors.

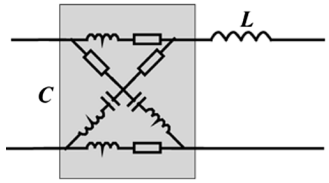

Fig. 15. Application for a Γ type EMI filter.

prevent the couplings between capacitors and the inductor [4]. Measures must be taken to reduce parasitic couplings [4], [5]. For example, for a typical two-winding inductor of EMI filters, the inductor windings are proposed to rotate by 90° to greatly reduce the coupling between the inductor and capacitors [4], [5]. When the couplings are minimized, the EMI filter performance can be further improved through the reduction of capacitor parasitics.

In Fig. 16, three Γ-type filters are measured. The first one is a Γ-type filter whose capacitor is composed of two parallel capacitors. The measured insertion voltage gain is the curve named base. The difference between the first and the second one is that, the couplings between inductor and capacitors are minimized for the second one. The last one is with both minimized couplings and ESL cancellation. The self-resonance frequency of the capacitor is 2 MHz. From Fig. 16, after the coupling between the inductor and capacitors are reduced, filter performance is significantly improved above 1 MHz. After ESL is cancelled, the filter performance is further improved. There is 30 dB at 20 MHz, and 20 dB at 30 MHz improvement achieved. For the

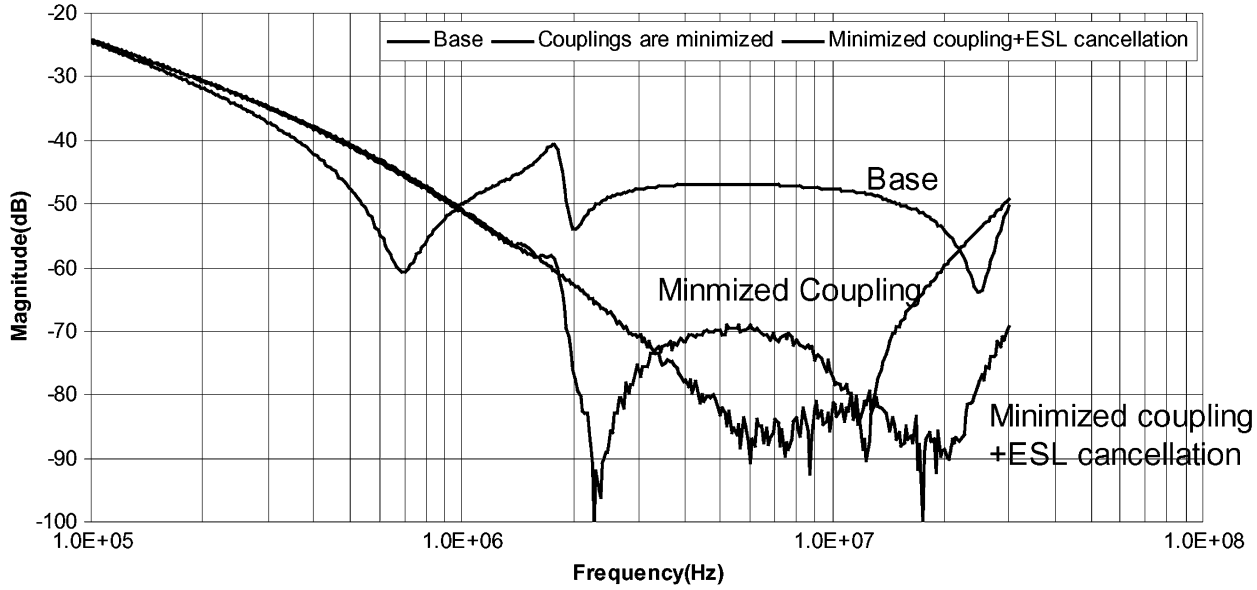

Fig. 16. Comparison of insertion voltage gains for a Γ-type filter.

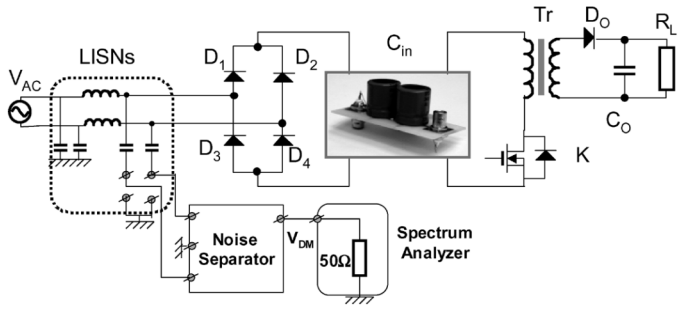

Fig. 17. DM noise measurement setup for the prototype with electrolytic capacitors.

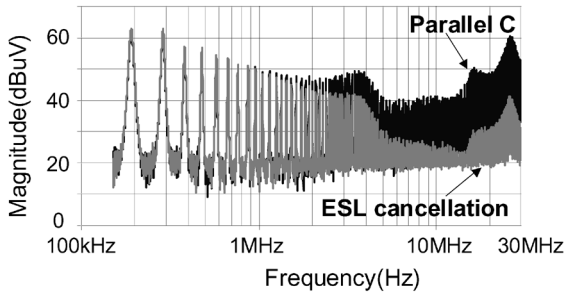

Fig. 18. Improvement of noise reduction due to ESL cancellation.

filter without ESL cancellation, the effects of ESL are obvious at around 2 MHz. On the contrary, for the filter with ESL cancellation, there is no resonance observed around 2 MHz and the insertion voltage gain goes down to a higher attenuation as frequency increases.

Based on these experiments, the proposed method is easily implemented in practical PCB layouts and can drastically improve the capacitor performance. It should be pointed out that the proposed cancellation method employs a balanced network structure. That means it would not cause any unbalanced problems such as the transformation between CM and DM noises.

IV. EMI Reduction for Practical Converters

Both the prototypes with electrolytic and film capacitors are tested in practical converters. Fig. 17 shows a differential mode (DM) noise measurement setup for a flyback converter with a switching frequency of 95 kHz. In Fig. 17, the line impedance stabilization network (LISN) is terminated by the 50-Ω input impedances of a noise separator [6]. The noise separator separates the DM noise and then the DM noise is measured using an EMC analyzer, Agilent E7402A.

The measurement is carried out by two steps. For the first step, DM noise is measured when the input energy tank capacitor $C_{\rm in}$ is two parallel electrolytic capacitors $(220\ \mu{\rm F}/250\ {\rm V})$. For the second step, the $C_{\rm in}$ is replaced with the prototype in Fig. 9 and then the DM noise is measured. The measured DM noise is compared in Fig. 18.

In Fig. 18, the DM noise using the prototype is much lower than that using two parallel capacitors in a very broad frequency range: 1–30 MHz. At 30 MHz, 20 dBμV (a factor of 10) improvement is achieved. This verified that the proposed ESL cancellation technique can significantly improve the capacitor's HF performance.

A similar experiment for the prototype with film capacitors is carried out in Fig. 19 for a 6-kW chopper circuit. DM noise is first measured when the decoupling capacitor C_1 is two parallel film capacitors. For the second step, the DM noise is measured after C_1 is replaced by a prototype with ESL cancellation. The measured DM noise is compared in Fig. 20.

In Fig. 20, the measured DM noise with ESL cancellation is much lower than that without ESL cancellation from 3–30 MHz. Up to 20 dBμV improvement is achieved due to the ESL cancellation. The background noise for this measurement is 60 dBμV.

These experiments clearly show that the proposed ESL cancellation technique can greatly improve the capacitor's filtering

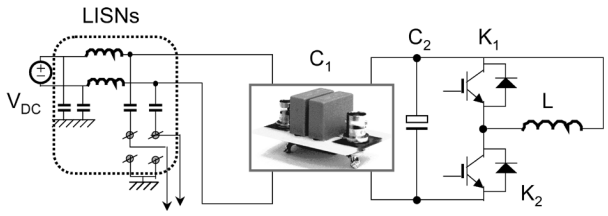

Fig. 19. DM noise measurement setup for a prototype with film capacitors.

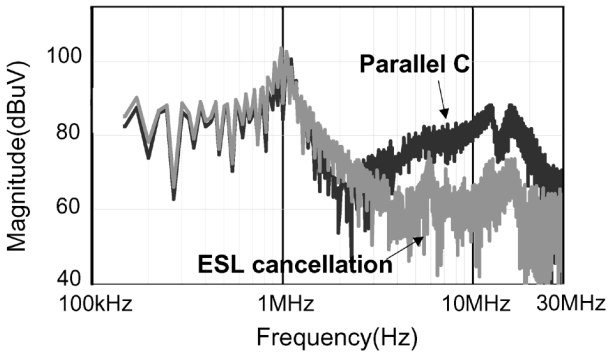

Fig. 20. Improvement of noise reduction due to ESL cancellation.

performance. It therefore promises higher noise reduction at high frequencies. The experiments also show that the capacitors with ESL cancellation have the same performance as parallel capacitors at low frequencies.

V. Conclusion

In this paper, a novel method is proposed to reduce the ESL and ESR of capacitors. The idea is implemented in prototypes for both film and electrolytic capacitors. The small-signal measurements are carried out in both frequency and time domains to verify the proposed technique. Finally, the technique is applied to practical power converters. The EMI noise measurement proves that the filtering performance of capacitors is greatly enhanced. As a result, the EMI noise is significantly reduced at high frequencies. This technique considerably broadens the effective operating frequency range of capacitors. It would be very useful for the reduction of EMI and HF voltage ripple.

Acknowledgment

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References

[1] M. A. Bueno and A. K. T. Assis, *J. Phys. D: Appl.*, vol. 28, p. 1802, 1995.

[2] N. Balabanian and T. Bickart, *Linear Network Theory: Analysis, Properties, Design and Synthesis*. York, PA: Matrix Publishers, Inc., 1981.

[3] L. Zhao and J. D. Van Wyk, "A generalized two conductor model for integrated passive components," in *Proc. CPES Sem.*, Blacksburg, Apr. 14–18, 2002, pp. 428–433.

[4] S. Wang, F. C. Lee, D. Y. Chen, and W. G. Odendaal, "Effects of parasitic parameters on EMI filter performance," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 869–877, May 2004.

[5] S. Wang, F. C. Lee, and W. G. Odendaal, "Controlling the parasitic parameters to improve EMI filter performance," in *Proc. IEEE Appl. Power Electron. Conf.*, Anaheim, CA, Feb. 22–26, 2004, vol. 1, pp. 503–509.

[6] ——, "Characterization, evaluation, and design of noise separator for conducted EMI noise diagnosis," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 974–982, Jul. 2005.

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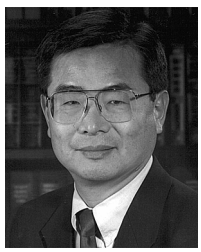

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